REMARKS

Reconsideration of the application is requested.

Claims 1, 6-10, 13, 15 and 19-26 are now in the application. Claims 1, 6-10, 13, 15 and 19-26 are subject to examination. Claims 1, 6-8, 13 and 15 have been amended. Claims 19-26 have been added. Claims 2-5, 11-12, 14 and 16-18 have been canceled to facilitate prosecution of the instant application.

Under the heading "Claim Objections" on page 2 of the above-identified Office Action, the Examiner objected to claim 8 because of one informality. Claim 8 has been amended with the term "are" to overcome the rejection.

Under the heading "Claim Rejections - 35 USC § 102" on pages 2-3 of the above-identified Office Action, claims 1, 4, 5, 12, 13, 16 and 18 have been rejected as being fully anticipated by an article entitled "Shifted Sideband Beamformer" by Pridham et al. (hereinafter Pridham) under 35 U.S.C. § 102.

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found as now

described and arguments in support of patentability are argued thereafter.

Amended claim 1 is a combination of original claims 1 and 3 in which the conversion device is realized by a multiplexer for multiplexing the K digital signals. The following additional modifications have been introduced in amended claim 1:

The wording "K" being greater than 1" can be inferred from the wording of original claim 1 because original claim 1 states that K and N are integers greater than 0 and that N is smaller than K.

The phrase "the digital filter device having memory elements formed by shift registers of length K" is disclosed on page 15, lines 6 to 8, of the specification of the instant application.

Claims 2 to 5 have been cancelled.

Claims 6 to 8 have been amended to be compatible with amended claim 1.

Claims 11 and 12 have been cancelled.

Claim 13 has been amended with the features of claim 14.

Claim 14 has been canceled.

Amended claim 15 is based on amended claim 1.

Claims 16-18 have been canceled.

New independent claim 19 covers the second embodiment of the invention shown in Fig. 5 and is derived from a combination of original claims 1, 4 and 5. Further, the function of the zero-inserting element ("insert K-1 zeros per sampling value of the digital signal into the digital signal") has been added. This feature is disclosed on page 16, lines 2 to 7, of the specification.

Further, analogously to amended claim 1, new claim 19, requires "K being greater than 1". Finally, the feature that the digital filter device has "memory elements formed by shift registers of length K" is disclosed on page 16, lines 12 to 15, of the specification.

New claims 20 to 24 are derived from original claims 6 to 10, respectively.

New claim 25 is derived from a combination of original claims 13 and 14.

New claim 26 is derived from original claim 15.

The common concept underlying the circuit of the instant application, as defined in independent claims 1 and 19, is to process K simultaneously received input signals by virtue of a suitable signal preprocessing (multiplexing in claim 1 or an introduction of zeros in claim 19) in such a manner that they can commonly be filtered in a specific filtering device. To this end, the digital filtering device contains memory elements, the length thereof corresponds to the number K of the signals to be filtered. It is this measure which provides for the common processing of the K input signals to be filtered in a common digital filtering device.

Pridham discloses a receiver for beamforming a number of analog receptions signal. As it is displayed in Figs. 5 and 13, the circuit contains for each input signal an analog/digital converter. The digital signals output by the analog/digital converters are combined in a complex digital beamformer unit. The combined signal output by the complex digital beamformer unit is filtered (per I and Q components) in low-pass filters connected to the output of the complex

digital beamformer unit.

Pridham fails to disclose that the low-pass filters have memory elements formed by shift registers of length K. Therefore, amended claims 1 and 19 of the instant application distinguish in a novel and inventive manner over Pridham.

Further, Pridham does not disclose any signal preprocessing or "conversion" for the preparation of K digital signals in order to be filtered by such a specific digital filter device: amended claim 1 requires a multiplexer for pre-processing the K digital signals before filtering. Pridham fails to disclose a multiplexer in the complex digital beam-former unit.

New claim 19 requires, as a signal preprocessing unit, a stage containing digital zero-inserting elements that are connected in parallel, whereby each zero-inserting element is fed with one of the digital signals and inserts K-1 zeros per sampling value of the digital signal into the digital signal. The zero pad unit illustrated in Fig. 13 of Pridham is not disclosed to insert K-1 zeros per sampling value into each digital signal (and from a technical point of view, there is no reason to insert K-1 zeros per sampling values into each digital signal, because the following low-pass filters do not

have the structure as required in new claim 19, i.e. the memory elements thereof are not formed by shift registers of length K).

Pridham also fails to disclose the signal preprocessing for filtering (i.e. multiplexing or K-1 zero insertion) as required in independent claims 1 and 19, respectively, and fails to disclose the structure of the digital filter device (i.e. memory elements formed by shift registers of length K). Therefore, Pridham fails to anticipate or suggest the teachings of amended claim 1 and new claim 19.

In items 8-11 on page 3 of the above-identified Office Action, claims 1, 2, 9, 10, 15, and 16 have been rejected as being fully anticipated by U.S. patent No. 5,712,879 to Tatsuta et al. (hereinafter Tatsuta) under 35 U.S.C. § 102.

Tatsuta discloses a signal adding device containing two analog/digital converters (Figs. 7, 8), a combiner 11, 29 for combining the digitized signals and a low-pass filter 4, 31 for filtering the combined signal. In Tatsuta, the low-pass filter is of a conventional type, i.e. the memory elements thereof <u>are not formed by shift registers of length K</u> (i.e. the number of signals to be filtered) as recited in claims 1 and 19 of the instant application.

In items 12-15 on page 4 of the above-identified Office Action, claims 1, 2, 11, 13, and 16 have been rejected as being fully anticipated by U.S. patent No. 5,544,128 to Kim et al. (hereinafter Kim) under 35 U.S.C. § 102.

Kim discloses a multi-beam digital beamforming apparatus containing N parallel summing paths each including an analog to digital converter, and a filter 90 downstream from the analog/digital converters. Kim fails to disclose the specific filtering device structure as defined in claims 1 and 19 of the instant application.

Under the heading "Claim Rejections - 35 USC § 103" on pages 4-5 of the above-identified Office Action, claims 3, 6, 7, 13, 14 and 17 have been rejected as being obvious over at least one of Tatsuta et al. (hereinafter Tatsuta), U.S. Patent No. 6,272,181 to Matt (hereinafter Matt), Pridham and/or U.S. Patent 6,314,147 to Liang under 35 U.S.C. § 103.

Matt discloses a device for aggregation of digital signals containing a multiplex unit 11, 21 for generating a composite multiplexed signal and a digital low-pass filter 12, 22 arranged downstream of the multiplex unit 11, 21. Matt fails to disclose that the digital low-pass filter 12, 22 has

memory elements constituted by shift registers of length L (e.g. the number *of* signals aggregated in the multiplexed signal). Therefore, Matt fails to anticipate or suggest the subject matter of new claim 1.

Claims 3, 6, 7, and 13 are based on amended claim 1, claim 1 is believed to be allowable and therefore claims 3, 6, 7 and 13 are also believed to be allowable.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 19. Claims 1 and 19 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 19.

Finally, applicants appreciatively acknowledge the Examiner's statement that claim 8 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicants respectfully believe that rewriting of claim 8 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1, 6-10, 13, 15 and 19-26 are solicited.

Please find enclosed a credit card authorization for $200.00 for the fourth independent claim.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicants

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